Oscillators and timers

Most electronics include some form of an oscillator or a timer, these can be pulsed, sinusoidal, square, sawtooth, or triangular shaped waveforms. The sources include clocks, crystals, RC discharges, filters etc. Here we will touch on some of the most basic and useful.

We have already seen that unijunctions can form the basis of an oscillator (with a charging capacitor). In general any non-linear element be be made to oscillate.
This square wave oscillator uses positive feedback to drive the op amp to its rails. The capacitor’s charging moves the non-inverting voltage past the threshold value and thus causes the device to switch states.

It is convenient to set $R_- = R_g$ so that the switching voltage is 1/2 the rail. The time constant for charging the capacitor, $1/R_C$, sets the frequency.

$$f = 2.2R_gC$$

This is a problem that we gave on the homework, so we will not solve it completely here. Note (1) that the output will be either + or - $V_{cc}$, (2) that there is positive feedback, so there is a hysteresis, and (3) that the capacitor will be charged in the direction of $V_{out}$. 
As the capacitor charges the output switches and the state swaps back and forth. The interest for us here is that the charging of a capacitor provides a useful time constant for setting a frequency. So we can imagine having a 2 state system that is a combination of a switch and the timing generated via a capacitor to build an oscillator.
The 555 set of chips is exactly this. It is a combination of digital logic (so a simple 2 state device), with an analog input to measure the charge on an external capacitor, and a low impedance (modest current) pathway for discharging the capacitor. Notice that the op amps are set as comparators with voltages of 1/3 and 2/3 Vcc. The digital circuit corresponds to a “set/reset flip-flop” - we’ll explain in the next slides, and that the output of the flip flop turns on the BJT (the discharge path of the capacitor. The way the circuit will work, is that the external capacitor will charge until it reaches 2/3 Vcc, then the upper op amp will switch states. This flips the flip flop which triggers the BJT to discharge the capacitor. The capacitor continues to discharge until it reaches 1/3 Vcc when the lower op amp changes state and the BJT is turned off. Then the process repeats.
Before we discuss the flip flop we introduce the “OR” gate whose output is high if either input (or both) is high. Otherwise the output is low.

The small circle on the “NOR” carries out a functional “NOT” to the output and thus inverts the output states.

The tables are called truth tables and provide the correspondence between the input and output states.

Since this is digital logic there are only two possible states
1, high, 5V
Or
0, low, 0V

Also 5 and 0 volts are just fictions and the actual values depend on the class of transistors that make up the logic circuit. But they serve as a first approximation.
The set/reset flip flop can be made up of 2 NOR gates wired as shown. The idea of a flip flop is that it is a two state device which can be set or reset depending on the inputs. Looking at the truth table, the flip flop is set when S is high and R is low. Then if S is sent low the flip flop keeps that state. Likewise if the flip flop was reset by having R high and S low again when R went low the flip flop would keep that state. Follow through the logic with the NORs to see how this works.
Demo Flip Flop #3

Now, switch S to 0
- R,0 stays high since both inputs low
- S,1 low since S is high

Now, switch R to 1
- R,1 low
- S,0 high
- Switches to low since at least 1 input is high
- Switches to high since both inputs are low

Now, switch S to 0
- R,0 stays high since both inputs low
- S,0 low since S is high

Now, switch R to 1
- R,1 low
- S,0 high
- Switches to low since at least 1 input is high
- Switches to high since both inputs are low
Brief introduction to the SR flip-flop

The SR flip flop is the simplest data storage device, and can be thought of as a latch. It has the following truth table.

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>( \bar{Q} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q</td>
<td>( \bar{Q} )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

To use the flip flop as a latch, set it and then put both S&R low. This holds the state until either S or R is switched. The lower pin is an enable pin that forces \( \bar{Q} \) low.

This just says the same thing, but it is interesting to think of the flip flop as a primitive storage device - although it is much more complicated than one would want to use today.
The use of the 555 as an oscillator (an astable) requires hooking up an external capacitor and a couple of resistors to have a pathway for charging and discharging. Notice how the op amps are connected, the S op amp is connected to be high when the capacitor voltage is less than 1/3 Vcc, the R op amp is connected to be high when the capacitor voltage is greater than 2/3 Vcc. In between 1/3 and 2/3 Vcc both R and S are low, so the flip flop holds the last outputs. The capacitor charges through R1 and R2 until it reaches 2/3 Vcc, then the flip flop resets, sending the inverting output high. This turns on the BJT which discharges the capacitor through R2 (note, R1 is out of the circuit). As the capacitor discharges R goes back low, and the flip flop is set again when it reaches 1/3 Vcc. The output is an inverted version of the digital signal that drives the discharging transistor.
6.071 Oscillators

Astable wave forms

\[ V_{\text{cap}}^{\text{up}} = V_{cc} \left[ 1 - e^{-t/(CR_1)} \right] \]

\[ V_{\text{cap}}^{\text{down}} = \frac{2V_{cc}}{3} e^{-t/CR_2} \]

\[ V_{\text{cap}}^{\text{up}} = \frac{1}{3} V_{cc} \]

\[ t_0 = C(R_1 + R_2) \ln \left( \frac{3}{2} \right) \]

\[ V_{\text{cap}}^{\text{up}} = \frac{2}{3} V_{cc}, t_1 = C(R_1 + R_2) \ln(3) \]

\[ t_{\text{on}} = t_1 - t_0 \]

\[ t_{\text{off}} = CR_2 \ln(2) \]

\[ \text{period} = t_{\text{on}} + t_{\text{off}} = C[(R_1 + 2R_2) \ln(2)] \]

\[ \text{dutycycle} = \frac{t_{\text{on}}}{\text{period}} = \frac{R_1 + R_2}{R_1 + 2R_2} \]

This busy figure shows the two separate rates for charging and discharging of the capacitor, and then calculates the time taken to charge and discharge. Notice that by adjusting R1 and R2 one can set both the frequency and the dutycycle.

The dutycycle is the fraction of time that the output is high.
A summary of the previous results. Since the charge path includes both resistors the time constant is longer and the duty cycle can not be set to 0.5. Of course we can not short R1 directly since then the supply Vcc would be pulled to ground when the transistor was turned on.
A simple demo where the charging resistor is made variable and the discharging resistor is set to 10 k. If both were 10 k then with the 0.01 µF cap the period should be about 0.21 ms and the frequency 4.8 kHz. The duty cycle should be about 0.67.
Demo Astable (cont.)

Period = C[(R₁ + R₂) \cdot \ln(2)]
= 10^{-8} \cdot 30,000 
= 0.21\text{ms} 
\downarrow 
\begin{align*}
f &= \frac{1}{\text{Period}} \\
&= \frac{1}{0.21\text{ms}} \\
&= 4.86\text{Hz} 
\end{align*}

\begin{align*}
\text{duty cycle} &= \frac{R₁ + R₂}{R₁ + 2R₂} \\
&= \frac{20,000}{30,000} \\
&= 0.67 
\end{align*}
To reduce the duty cycle to less than 50% we need to separate the charging and discharging pathways. This is conveniently achieved by shorting out R2 during the charging stage. Now the capacitor charges through R1 and discharges through R2, and we can make the duty cycle as low as we wish.
The 555 can also be used to generate a triggered pulse of a specific duration. When the trigger is pulled low, S goes low and the flip flop is set. This leads to a charging of the capacitor (through R₁), (and an output pulse) until the capacitor voltage reaches 2/3Vcc.

The 10k resistor is just a pull-up.

The monostable (1 triggered pulse at a time) operation is achieved by separating the trigger input from the capacitor. Now when the trigger is pulled down the capacitor will charge until it reaches the 2/3 Vcc threshold at which point it will discharge. The capacitor will remain discharged until there is another trigger pulse. Recall that the action of the trigger is to reset the flip flop when its input is lower than 1/3 Vcc, so pin 6 must be actively pulled down to initiate another pulse.
Monostable waveforms

Once the capacitor starts charging it will continue until it reaches 2/3 of Vcc at which point it is discharged through the transistor.

\[ V_{cap}^{up} = V_{CC} \left[ 1 - e^{-t_{CR}/CR_1} \right] \]

The pulse on time is set by the charging rate,

\[ V_{cap}^{up} = \frac{2}{3} V_{CC} \]

\[ t_{on} = CR_1 \ln(3) \]

The wave forms showing the action of the 555 as a monostable. Notice that the discharge is fast since it is not limited by a series resistor (just the resistance of the BJT).
A demo showing the monostable action of the 555. Notice that a BJT has been used to invert the trigger pulse. When Vin is high pin 2 is pulled low and when Vin is low pin 2 is set high.
If the resistor is set to 10 k then the pulse length should be about 110 µs.
The 555 provides a periodic pulse which is converted to a current pulse by the transistor. The 220 Ω resistor is to limit the power delivered to the LED.

An overly complicated way of making a flashing light, but it works.
There are a variety of 555 chips based on bipolar transistors, CMOS or a combination. The bipolar typically are typically slower, require higher supply voltages yet can provide higher output currents.

<table>
<thead>
<tr>
<th>Type</th>
<th>Supply min V</th>
<th>Supply max V</th>
<th>Trigger µA</th>
<th>Frequency max MHz</th>
<th>Source mA</th>
<th>Sink mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN555</td>
<td>4.5</td>
<td>18</td>
<td>3000</td>
<td>0.5</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>ICL7555</td>
<td>2</td>
<td>18</td>
<td>60</td>
<td>&lt;10</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>LMC555</td>
<td>2</td>
<td>18</td>
<td>170</td>
<td>0.01</td>
<td>10</td>
<td>100</td>
</tr>
</tbody>
</table>
**555 datasheet #1**

**LM555/NE555/SA555**

**Single Timer**

**Features**
- High Current Drive Capability (25mA)
- Adjustable Delay (10ms - 20s)
- Temperature Stability ±0.01% per °C
- Optimal from ±5V to ±15V
- Turn Off Time Less Than 30μsec

**Applications**
- Precision Timing
- Pulse Formation
- Waveform Generation
- Sequential Timing

**Description**
LM555/NE555/SA555 is a highly versatile monolithic integrated circuit capable of producing accurate timing pulses. With its versatile operation, the time delay is controlled by one or two external resistor and capacitor. With its adjustable power supply frequency and duty cycle, it is accurately controlled with two external resistors and one capacitor.
555 datasheet #2

Internal Block Diagram

- GND
- Trigger
- Output
- Reset
- Ver
- Bz
- Over
- Threshold
- Control Voltage

Slide 21
### 555 Datasheet #3

#### Absolute Maximum Ratings (TA = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VCC</td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>Max Temperature (stressing)</td>
<td>TSTG</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Pd</td>
<td>1500</td>
<td>mW</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>TstS</td>
<td>0 to 70</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Tô</td>
<td>-40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>Range Temperature Range</td>
<td>TôH</td>
<td>-150 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

#### Electrical Characteristics

- **Notation:** 
  - TA = 25°C
  - VCC = 5V
  - Unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VCC</td>
<td></td>
<td>4.5</td>
<td>5.0</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>Supply Current (maximum)</td>
<td>Icc</td>
<td></td>
<td>2.0</td>
<td>6.0</td>
<td>8.0</td>
<td>mA</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>VIN</td>
<td></td>
<td>2.0</td>
<td>5.5</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>Output Current (maximum)</td>
<td>Icc</td>
<td></td>
<td>1.0</td>
<td>1.4</td>
<td>1.6</td>
<td>A</td>
</tr>
</tbody>
</table>

### 6.071 Oscillators

22
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Notes</th>
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</thead>
<tbody>
<tr>
<td>555 datasheet #4</td>
<td></td>
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</tr>
<tr>
<td>Application Information</td>
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<tr>
<td>6.071 Oscillators</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 1: Basic Operating Table</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Current</td>
<td>5.85</td>
<td>mA</td>
</tr>
<tr>
<td>Trigger Voltage</td>
<td>5.85</td>
<td>V</td>
</tr>
<tr>
<td>Trigger Current</td>
<td>5.85</td>
<td>mA</td>
</tr>
<tr>
<td>Reset Voltage</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Power Supply</td>
<td>5.85</td>
<td>mA</td>
</tr>
<tr>
<td>Low Current Inhibit</td>
<td>5.85</td>
<td>mA</td>
</tr>
<tr>
<td>High Current Inhibit</td>
<td>5.85</td>
<td>mA</td>
</tr>
<tr>
<td>Stand-by Power</td>
<td>5.85</td>
<td>mA</td>
</tr>
<tr>
<td>Stand-by Current</td>
<td>5.85</td>
<td>mA</td>
</tr>
<tr>
<td>Stand-by Voltage</td>
<td>5.85</td>
<td>V</td>
</tr>
</tbody>
</table>

Note: All data points represent the 555 datasheet information in the range of the specified voltage.
LC oscillators

So far we have looked at RC oscillators which work well at low frequency provided that great stability is not necessary. LC oscillators are preferred at high frequencies and since the Q can be several hundred, the stability is improved.

Until recently op amps did not reach high enough frequencies to be used with LC oscillators, but today op amps with 500 MHz 3 dB frequencies are available, and we will restrict ourselves to these.

The simplest method of generating an oscillator is then to use positive feedback and rely on an LC filter in the feedback path to select the desired frequency.
An LC oscillator essentially uses a frequency selective, positive feedback to drive the op amp into oscillation (from rail to rail). The tank circuit is a high impedance to ground for its resonance frequency,

\[ f = \frac{1}{2\pi \sqrt{LC}} \]

and a short otherwise. Since the output is a square-wave, all even harmonics of the resonance frequency are also generated.
There is rather limited quality factor, $Q$, for an LC oscillator (~200), but with crystals $Q$s of 100,000 are possible. The equivalent circuit for an piezoelectric quartz crystal is:

The resonance condition is given by the upper (motion) arm. For a 10 MHz crystal a typical value for the inductor is $L = 9.8 \, \text{mH}$, leading to a very low capacitance and very high stored energy. The crystal looks like a band pass filter.